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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/394,302 | 09/10/1999 | ALVAR A. DEAN | BU9-98-062 | 4030 |

29154 7590 01/29/2003

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| EXAMINER |
|---|
| MCGRATH, CHRISTOPHER R |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2184 | |

DATE MAILED: 01/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/394,302 | DEAN ET AL. | |
| | Examiner | Art Unit | |
| | Christopher R McGrath | 2184 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *55-83* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *55-70* is/are allowed.

6)☒ Claim(s) *71-83* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *09 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Drawings*

1.0 The proposed drawing correction and/or the proposed substitute sheets of drawings, filed on December 9, 2003 have been accepted. A proper drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The correction to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 71, 72, 74, and 77 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy U.S. Patent No. 6,480,978 in view of Akram U.S. Patent No. 6,119,255.

2.0 Referring to claim 71, the applied reference Roy discloses an integrated circuit chip test board adapted to test integrated circuit chips. As per the limitation where the test device comprises sockets on the test board adapted to hold integrated circuit chips to be tested, the applied reference Roy does not teach this limitation. The Akram reference teaches (column 3, lines 24-25) receptacles that comprise sockets attached to a test board that are sized to receive an integrated circuit. When the invention was made, it would have been obvious to one of ordinary skill in the art to of included the sockets as taught by the Akram reference in the test board in the

Roy reference. This would have been obvious because the Akram reference teaches (column 2, lines 58-64) that the receptacles are coupled to the test circuitry and to a power supply to provide power the circuit under test.

2.1 As per the limitation where the device includes testing circuitry on the test board electronically connected to the sockets that includes comparators arranged in parallel and electrically connected to the sockets and where the circuitry identifies a defective integrated circuit as having a different output when compared to the other outputs, the applied reference Roy as altered discloses (column 7, lines 45-58 and Fig. 8) a comparison circuit that comprises a number of XOR gates arranged in parallel that receives data from the DTUs and compares this data to identify bit errors.

3.0 Referring to claim 72, the applied reference Roy discloses (column 3, lines 23-24) that the DUTs are normally similar or preferably identical devices. In the Roy reference the DTUs are equivalent to the integrated circuit chips as defined by the applicant.

4.0 Referring to claim 74, the limitation where the test device further comprises a memory attached to the test board where the memory is adapted to store test results, the applied reference Roy discloses (column 6, lines 10-12 and Fig. 3) that an Error Memory is used to collect error data.

5.0 Referring to claim 77, the limitation wherein by comparing whether outputs of all integrated circuit chips are identical, the testing circuit does not require a specific proper output that a given input should produce for a specific design of the integrated circuit chip being tested, the applied reference Roy discloses (column 7, lines 45-58 and Fig. 8) a comparison circuit that comprises a number of XOR gates arranged in parallel that receives data from the DTUs and

compares this data to identify bit errors. This type of comparison circuit does not require a specific proper output that a given input should produce for a specific design of the integrated circuit chip being tested.

Claim 73 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roy in view of Akram as applied to claim 71 above, and further in view of Stoner U.S. Patent No. 4,768,195.

6.0 Referring to claim 73, the Roy reference as altered teaches the limitations of claim 71, but fails to teach the limitation where the test device further comprises visual test failure indicators attached to the test board such that one of the visual test indicators is adjacent each of the sockets. The Stoner reference discloses (column 6, lines 46-51 and Fig. 1) decimals, which are lights that are used as visible indicator to indicate passing or falling chips in an integrated circuit test system. When the invention was made, it would have been obvious to one of ordinary skill in the art to of included the decimals as taught by the Stoner reference in the test board in the Roy reference as altered and to of placed the decimals adjacent to each of the sockets. This would have been obvious because the Stoner reference teaches (column 6, lines 40-51) that the decimal points indicate the number of errors detected.

Claims 75 and 76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy in view of Akram as applied to claim 71 above, and further in view of Franke U.S. Patent No. 4,122,995.

7.0 Referring to claim 75, the Roy reference as altered teaches the limitations of claim 71, but fails to teach the limitation where the test device further comprises a known good integrated

circuit chip attached to the board. The Franke reference discloses (column 1, line 64 to column 2, line 8) providing a standard unit in an integrated circuit test device. The standard unit in the Franke reference is equivalent to the known good integrated circuit chip as defined by the applicant. When the invention was made, it would have been obvious to one of ordinary skill in the art to of incorporated the standard unit as taught by the Franke reference into the test device in the Roy reference as altered. This would have been obvious because the Roy reference teaches (column 6, lines 16-22) that the interface circuitry can be configured to operate in different modes including one that includes testing integrated circuit devices using a known good device to generate an expected response.

8.0 Referring to claim 76, the Roy reference as altered teaches the limitations of claim 71, but fails to teach the limitation where all of the comparators are connected to the known good integrated circuit chip such that any integrated circuit chips that produce an output different than the output produced by the known good integrated circuit chip is identified as a defective integrated circuit chip. The Franke reference teaches (column 1, line 64 to column 2, line 8) that the output of the unit to be tested is compared to the standard unit to identify if the unit to be tested is faulty. When the invention was made, it would have been obvious to one of ordinary skill in the art to of incorporated a standard unit as taught by the Franke reference into the test device in the Roy reference as altered and to of compared the output of the unit to be tested to the standard unit. This would have been obvious because the Roy reference teaches (column 6, lines 16-22) that the interface circuitry can be configured to operate in different modes including one that includes testing integrated circuit devices using a known good device to generate an expected response.

Claims 78, 79, and 81-83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Roy U.S. Patent No. 6,480,978 in view of Akram U.S. Patent No. 6,119,255, and further in view of Franke U.S. Patent No. 4,122,995.

9.0 Referring to claim 78, the applied reference Roy discloses an integrated circuit chip test board adapted to test integrated circuit chips. As per the limitation where the test device comprises sockets on the test board adapted to hold integrated circuit chips to be tested, the applied reference Roy does not teach this limitation. The Akram reference teaches (column 3, lines 24-25) receptacles that comprise sockets attached to a test board that are sized to receive an integrated circuit. When the invention was made, it would have been obvious to one of ordinary skill in the art to of included the sockets as taught by the Akram reference in the test board in the Roy reference. This would have been obvious because the Akram reference teaches (column 2, lines 58-64) that the receptacles are coupled to the test circuitry and to a power supply to provide power the circuit under test.

9.1 As per the limitation where the device includes testing circuitry on the test board electronically connected to the sockets that includes comparators arranged in parallel and electrically connected to the sockets and where the circuitry identifies a defective integrated circuit as having a different output when compared to the other outputs, the applied reference Roy as altered discloses (column 7, lines 45-58 and Fig. 8) a comparison circuit that comprises a number of XOR gates arranged in parallel that receives data from the DTUs and compares this data to identify bit errors.

9.2 The Roy reference as altered teach the above limitations, but fails to teach the limitation where the test device further comprises a golden socket for a known good circuit chip attached to the board. The Franke reference discloses (column 1, line 64 to column 2, line 8) providing a standard unit in an integrated circuit test device. The standard unit in the Franke reference is equivalent to the known good integrated circuit chip as defined by the applicant. When the invention was made, it would have been obvious to one of ordinary skill in the art to of incorporated the standard unit as taught by the Franke reference into the test device in the Roy reference as altered and to of included a golden socket in the test device for the standard unit. This would have been obvious because the Roy reference teaches (column 6, lines 16-22) that the interface circuitry can be configured to operate in different modes including one that includes testing integrated circuit devices using a known good device to generate an expected response.

10.0 Referring to claim 79, the applied reference Roy discloses (column 3, lines 23-24) that the DUTs are normally similar or preferably identical devices. In the Roy reference the DTUs are equivalent to the integrated circuit chips as defined by the applicant.

11.0 Referring to claim 81, the limitation where the test device further comprises a memory attached to the test board where the memory is adapted to store test results, the applied reference Roy discloses (column 6, lines 10-12 and Fig. 3) that an Error Memory is used to collect error data.

12.0 Referring to claim 82, the Roy reference as altered teaches the limitations of claim 78, but fails to teach the limitation where all of the comparators are connected to the known good integrated circuit chip such that any integrated circuit chips that produce an output different than the output produced by the known good integrated circuit chip is identified as a defective

integrated circuit chip. The Franke reference teaches (column 1, line 64 to column 2, line 8) that the output of the unit to be tested is compared to the standard unit to identify if the unit to be tested is faulty. When the invention was made, it would have been obvious to one of ordinary skill in the art to of incorporated a standard unit as taught by the Franke reference into the test device in the Roy reference as altered and to of compared the output of the unit to be tested to the standard unit. This would have been obvious because the Roy reference teaches (column 6, lines 16-22) that the interface circuitry can be configured to operate in different modes including one that includes testing integrated circuit devices using a known good device to generate an expected response.

13.0 Referring to claim 83, the limitation wherein by comparing whether outputs of all integrated circuit chips are identical, the testing circuit does not require a specific proper output that a given input should produce for a specific design of the integrated circuit chip being tested, the applied reference Roy discloses (column 7, lines 45-58 and Fig. 8) a comparison circuit that comprises a number of XOR gates arranged in parallel that receives data from the DTUs and compares this data to identify bit errors. This type of comparison circuit does not require a specific proper output that a given input should produce for a specific design of the integrated circuit chip being tested.

Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Roy in view of Akram and Franke as applied to claim 78 above, and further in view of Stoner U.S. Patent No. 4,768,195.

14.0 Referring to claim 80, the Roy reference as altered teaches the limitations of claim 71, but fails to teach the limitation where the test device further comprises visual test failure indicators attached to the test board such that one of the visual test indicators is adjacent each of the sockets. The Stoner reference discloses (column 6, lines 46-51 and Fig. 1) decimals, which are lights that are used as visible indicator to indicate passing or falling chips in an integrated circuit test system. When the invention was made, it would have been obvious to one of ordinary skill in the art to of included the decimals as taught by the Stoner reference in the test board in the Roy reference as altered and to of placed the decimals adjacent to each of the sockets. This would have been obvious because the Stoner reference teaches (column 6, lines 40-51) that the decimal points indicate the number of errors detected.

***Allowable Subject Matter***

Claims 55-70 are allowed.

The following is an examiner's statement of reasons for allowance:

15.0 Claim 55 and the corresponding dependent claims 56-62 are considered to contain allowable subject matter by the examiner due to the limitations in claim 55 where the transportable integrated circuit chip test device comprises a transportable test box, where a plurality of test boards are mounted in the test box, and a portable power supply is in the test box connected to the test boards. The prior art does not include or fairly suggest this limitation.

16.0 Claim 63 and the corresponding dependent claims 64-70 are considered to contain allowable subject matter by the examiner due to the limitations in claim 63 where the transportable integrated circuit chip test device adapted to test ASCI chips comprises a

transportable test box, where a plurality of test boards are mounted in the test box, and a portable power supply is in the test box connected to the test boards. The prior art does not include or fairly suggest this limitation.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

17.0 Any inquiry concerning this communication should be directed to Christopher R. McGrath at telephone number (703) 305-4897. The examiner can normally be reached Monday-Friday (7:30-5:00), alternate Fridays off.

If attempts to reach the examiner are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, can be reached at (703) 305-9713.

Any inquiry of a general nature or relating to the status of this application should be directed to the group receptionist, whose telephone number is (703) 305-3900.

**Any response to this action should be mailed to:**
Commissioner of Patents and Trademarks
Washington, DC 20231

**Or faxed to:**
(703) 746-7239, (for formal communications intended for entry)

**Or:**
(703) 746-7240, (for informal or draft communications, Please label "PROPOSED" OR "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Christopher R. McGrath
Examiner
Art Unit 2184

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100